UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/578,007	05/02/2006	Bo-Sung Kim	SAM-OPP052589US	6587

22150 7590 04/14/2009
F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
ROLAND, CHRISTOPHER M	
ART UNIT	PAPER NUMBER
2893	

MAIL DATE	DELIVERY MODE
04/14/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/578,007	KIM ET AL.	
	Examiner	Art Unit	
	Christopher M. Roland	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2008* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Amendment filed 24 December 2008 is acknowledged. **Claims 1, 5, 7, and 8** have been amended. **Claims 1, 2, and 4-9** are pending.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in the Republic of Korea on 7 February 2005. It is noted, however, that applicant has not filed a certified copy of the KR 10-2004-0008346 application as required by 35 U.S.C. 119(b).

Drawings

3. **The drawings** are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 182. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. **The abstract** of the disclosure is objected to because it has not been provided on a separate sheet consisting only said abstract. Applicant has instead filed the front page of the related PCT document as the abstract. The abstract must be filed on a separate sheet consisting only said abstract. Further, a patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains, not merely a recitation of the first independent claim as originally filed. Correction is required. See MPEP § 608.01(b).

5. **The disclosure** is objected to because of the following informalities: the specification contains numerous changes to the font and spacing therein. Appropriate correction is required.

6. **The title** of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: THIN FILM TRANSISTOR COMPRISING PARYLENE AS A DIELECTRIC LAYER.

Claim Objections

7. **Claims 1 and 5-8** are objected to because of the following informalities:

Claims 1, 5, 7, and 8 recite the limitation, "wherein at least one of the gate insulating layer and the passivation layer is made at least one of Parylene N, Parylene C, or Parylene D." This is believed to be merely a typographic error and that Applicant intends, "wherein at least one of the gate insulating layer and the passivation layer is made of at least one of Parylene N, Parylene C, or Parylene D."

Claim 6 recites the limitation, "wherein the gate insulating layer and the passivation layer is made of Parylene by chemical vapor deposition." This is inconsistent with claim 5, off which claim 6 depends, which recites, "wherein at least one of the gate insulating layer and the passivation layer is made at least one of Parylene N, Parylene C, or Parylene D." Examiner believes Applicant intends, ""wherein the at least one of the gate insulating layer and the passivation layer is made of Parylene by chemical vapor deposition."

Claims 7 and 8 recite the limitation, "the corresponding portion." There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 1, 2, and 4-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US Patent 6,100,954, hereinafter Kim '954) of record in view of Stephany et al. (US Patent 5,177,475, hereinafter Stephany '475).

With respect to claim 1, Kim '954 teaches (FIG. 15B) a thin film transistor array panel substantially as claimed, comprising:

a substrate (111) (col. 19, ln. 41 – col. 20, ln. 7);

a gate electrode (113) formed on the substrate (col. 19, ln. 41 – col. 20, ln. 7);

a gate insulating layer (157) covering the gate electrode and the substrate (col. 19, ln. 41 – col. 20, ln. 7);

a source electrode (123) and a drain electrode (127) formed on the gate insulating layer (col. 19, ln. 41 – col. 20, ln. 7);

a semiconductor layer (119) formed on the gate insulating layer and the source electrode and the drain electrode (col. 19, ln. 41 – col. 20, ln. 7); and

a passivation layer (159) covering the semiconductor layer, the source electrode, the drain electrode, and the gate insulating layer, wherein at least one of the gate insulating layer and the passivation layer is made of Parylene (col. 19, ln. 41 – col. 20, ln. 7).

Thus, Kim '954 is shown to teach all the features of the claim with the exception of wherein the at least one of the gate insulating layer and the passivation layer is made at least one of Parylene N, Parylene C, or Parylene D.

However, Stephany '475 teaches Parylene N applied over electrodes of a liquid crystal device using thin film transistors because of its low dissipation factor, high

dielectric strength, and a dielectric constant invariant with frequency (col. 10, ln. 4 - col. 11, ln. 14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the Parylene passivation layer of Kim '954 of Parylene N as taught by Stephany '475 as a dielectric having low dissipation factor, high dielectric strength, and a dielectric constant invariant with frequency.

Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

With respect to claim 2, Kim '954 teaches wherein the substrate is made of one material selected from plastic, glass, and metal (col. 19, ln. 41 – col. 20, ln. 7).

With respect to claim 4, Kim '954 teaches further comprising a pixel electrode (131) formed on the passivation layer and connected to the drain electrode through a contact hole of the passivation layer that exposes a portion of the drain electrode (col. 19, ln. 41 – col. 20, ln. 7).

With respect to claim 5, Kim '954 teaches (FIG. 15B) a manufacturing method of a thin film transistor array panel substantially as claimed, comprising:

forming a gate electrode (113) on a substrate (111) (col. 19, ln. 41 – col. 20, ln. 7);

forming a gate insulating layer (157) covering the gate electrode on the substrate (col. 19, ln. 41 – col. 20, ln. 7);

forming a source electrode (123) and a drain electrode (127) on the gate insulating layer (col. 19, ln. 41 – col. 20, ln. 7);

forming a semiconductor layer (119) covering the source electrode and a portion of the drain electrode (col. 19, ln. 41 – col. 20, ln. 7); and

forming a passivation layer (159) covering the gate insulating layer, the source electrode, the drain electrode, and the semiconductor layer, wherein at least one of the gate insulating layer and the passivation layer is made of Parylene (col. 19, ln. 41 – col. 20, ln. 7).

Thus, Kim '954 is shown to teach all the features of the claim with the exception of wherein the at least one of the gate insulating layer and the passivation layer is made at least one of Parylene N, Parylene C, or Parylene D.

However, Stephany '475 teaches Parylene N applied over electrodes of a liquid crystal device using thin film transistors because of its low dissipation factor, high dielectric strength, and a dielectric constant invariant with frequency (col. 10, ln. 4 - col. 11, ln. 14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the Parylene passivation layer of Kim '954 of Parylene N as taught by Stephany '475 as a dielectric having low dissipation factor, high dielectric strength, and a dielectric constant invariant with frequency.

Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

With respect to claim 6, Kim '954 teaches wherein the gate insulating layer and the passivation layer is made of Parylene by chemical vapor deposition (col. 9, ln. 9-34).

With respect to claim 7, Kim '954 teaches (FIG. 15) a thin film transistor substantially as claimed, comprising:

a substrate (111) (col. 19, ln. 41 – col. 20, ln. 7);

a gate electrode (113) formed on the substrate (col. 19, ln. 41 – col. 20, ln. 7);

a gate insulating layer (157) covering the substrate and the gate electrode (col. 19, ln. 41 – col. 20, ln. 7);

a semiconductor layer (119) formed on the gate insulating layer and disposed on the corresponding portion of the gate electrode (col. 19, ln. 41 – col. 20, ln. 7);

a source electrode (123) and a drain electrode (127) contacting portions of the semiconductor layer, formed on the gate insulating layer, and separated by a predetermined distance (col. 19, ln. 41 – col. 20, ln. 7); and

a passivation layer (159) covering the semiconductor layer, the gate insulating layer, the source electrode, and the drain electrode, wherein at least one of the gate insulating layer and the passivation layer is made of Parylene (col. 19, ln. 41 – col. 20, ln. 7).

Thus, Kim '954 is shown to teach all the features of the claim with the exception of wherein the at least one of the gate insulating layer and the passivation layer is made at least one of Parylene N, Parylene C, or Parylene D.

However, Stephany '475 teaches Parylene N applied over electrodes of a liquid crystal device using thin film transistors because of its low dissipation factor, high dielectric strength, and a dielectric constant invariant with frequency (col. 10, ln. 4 - col. 11, ln. 14)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the Parylene passivation layer of Kim '954 of Parylene N as taught by Stephany '475 as a dielectric having low dissipation factor, high dielectric strength, and a dielectric constant invariant with frequency.

Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

With respect to claim 8, Kim '954 teaches (FIG. 15C) a thin film transistor array panel substantially as claimed, comprising:

a substrate (111) (col. 19, ln. 41 – col. 20, ln. 7);

a source electrode (123) and a drain electrode (127) formed on the substrate and separated by a predetermined distance (col. 19, ln. 41 – col. 20, ln. 7);

a semiconductor layer (119) covering the source electrode and the drain electrode (col. 19, ln. 41 – col. 20, ln. 7);

a gate insulating layer (157) covering the substrate and the semiconductor layer (col. 19, ln. 41 – col. 20, ln. 7);

a gate electrode (113) formed on the gate insulating layer and disposed on the corresponding portion between the source electrode and the drain electrode (col. 19, ln. 41 – col. 20, ln. 7); and

a passivation layer (159) covering the gate insulating layer and the gate electrode, wherein at least one of the gate insulating layer and the passivation layer is made of Parylene (col. 19, ln. 41 – col. 20, ln. 7).

Thus, Kim '954 is shown to teach all the features of the claim with the exception of wherein the at least one of the gate insulating layer and the passivation layer is made at least one of Parylene N, Parylene C, or Parylene D.

However, Stephany '475 teaches Parylene N applied over electrodes of a liquid crystal device using thin film transistors because of its low dissipation factor, high dielectric strength, and a dielectric constant invariant with frequency (col. 10, ln. 4 - col. 11, ln. 14)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the Parylene passivation layer of Kim '954 of Parylene N as taught by Stephany '475 as a dielectric having low dissipation factor, high dielectric strength, and a dielectric constant invariant with frequency.

Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

With respect to claim 9, Kim '954 teaches further comprising a pixel electrode (131) formed on the passivation layer and connected to the drain electrode through a contact hole of the gate insulating layer and the passivation layer that exposes a portion of the drain electrode (col. 19, ln. 41 – col. 20, ln. 7).

Response to Arguments

9. Applicant's arguments filed 24 December 2008 have been fully considered but they are not persuasive.

Applicant argues (remarks, p. 5) That the prior art of record fails to teach or suggest the newly presented limitation of claims 1, 5, 7, and 8, "at least one of Parylene N, Parylene C or Parylene D." Examiner respectfully disagrees.

Stephany '475 is cited in the above rejection to address the newly presented limitation of claims 1, 5, 7, and 8.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Yamasaki (US Patent Application Publication 2004/0046902) teaches a thin film transistor comprising Parylene N as a dielectric layer.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher M. Roland whose telephone number is 571-270-1271. The examiner can normally be reached on Monday-Friday, 8:00AM-5:00PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. M. R./
Examiner, Art Unit 2893

/Davienne Monbleau/
Supervisory Patent Examiner, Art Unit 2893